

WHAT IS CLAIMED IS:

1. A semiconductor package for three-dimensional mounting comprising:

a first substrate having an upper surface on which a first metal pattern is formed and a lower surface on which a second metal pattern is formed, said first metal pattern and second metal pattern being electrically connected to each other;

a semiconductor chip which is placed on the upper surface of the first substrate and is electrically connected to the first metal pattern;

a sealing resin layer which is formed on the upper surface of the first substrate and seals the semiconductor chip and the first metal pattern;

a conductive wire which passes through the resin layer and has one end electrically connected to the first metal pattern and the other end exposed at a top surface of the resin layer; and

a first electrode which is formed on the lower surface of the first substrate and is electrically connected to the second metal pattern.

2. A semiconductor package according to claim 1, wherein a solder ball is bonded to at least one of the other end of the conductive wire and the first electrode.

3. A semiconductor package according to claim 1, further comprising a second substrate placed on the surface of the resin layer, having an upper surface and a lower surface opposite the upper surface, wherein the second substrate includes a third metal pattern which is electrically connected to the other end of the conductive wire from the lower surface of the second substrate, and a second electrode which is formed on the upper surface of the second substrate and is electrically connected to the third metal pattern.

4. A semiconductor package according to claim 3, wherein a solder ball is bonded to at least one of the first electrode at the first substrate and the second electrode at the second substrate.

5. A semiconductor package according to claim 1, further comprising:

a fourth metal pattern which is formed on the surface of the resin layer and is electrically connected to the other end of the conductive wire;

an insulating layer which covers the fourth metal pattern; and  
an third electrode which is exposed from the insulating layer and is electrically connected to the fourth metal pattern.

6. A semiconductor package according to claim 2, further comprising:

a fourth wiring pattern which is formed on the surface of the sealing resin layer and is electrically connected to the other end of the conductive wire;

an external insulating layer which covers the fourth wiring pattern; and

an upper surface connecting electrode which is located on or near the surface of the external insulating layer and is electrically connected to the fourth wiring pattern.

7. A semiconductor package according to claim 3, wherein the first electrode and the second electrode are disposed at different positions in horizontal directions.

8. A semiconductor package according to claim 7, wherein a second semiconductor chip is stacked on the upper surface of the second substrate, the second semiconductor chip being electrically connected to the second electrode and having a function different from that of the semiconductor chip.

9. A semiconductor package according to claim 5, wherein the first electrode and the third electrode are disposed at different positions in horizontal directions.

10. A semiconductor package according to claim 9, wherein a third semiconductor chip is stacked on the upper surface of the

second substrate, the third semiconductor chip being electrically connected to the third electrode and having a function different from that of the semiconductor chip.

11. A semiconductor device in which the semiconductor package for three-dimensional mounting of claim 1 is mounted on a mother board.

12. A semiconductor device in which a plurality of semiconductor packages of claim 1 are stacked.

13. A semiconductor device according to claim 12, wherein semiconductor chips of the semiconductor packages of the plurality of semiconductor packages, comprise memory elements.

14. A method of fabricating a semiconductor package for three-dimensional mounting, comprising:

(a) placing a semiconductor chip on an upper surface of a substrate, said substrate having the upper surface on which a first metal pattern is formed and a lower surface on which a second metal pattern is formed, said first metal pattern and second metal pattern being electrically connected to each other;

(b) electrically connecting the semiconductor chip and the first metal pattern to each other;

(c) sealing the semiconductor chip and the first metal pattern with sealing resin; and

(d) forming, in the sealing resin, a through hole which reaches the first metal pattern, and forming a wire inside the through hole to electrically connect to the first metal pattern.

15. A method according to claim 14, wherein the through hole is formed by irradiating a laser beam onto a predetermined position of the surface of the sealing resin.

16. A method of fabricating a semiconductor package for three-dimensional mounting, comprising:

(a) preparing a substrate;

(b) forming a first metal pattern on an upper surface of the substrate;

(c) forming a second metal pattern on a lower surface of the substrate;

(d) electrically connecting the first metal pattern and the second metal pattern to each other;

(e) placing a semiconductor chip on the upper surface of the substrate;

(f) electrically connecting the semiconductor chip and the first metal pattern to each other;

(g) sealing the semiconductor chip and the first metal pattern with sealing resin;

(h) forming a through hole extending from the surface of the sealing resin to the first metal pattern; and

(i) forming a wire inside the through hole.

17. A method according to claim 16, wherein the through hole is formed by irradiating a laser beam onto a predetermined position of the surface of the sealing resin.

18. A method according to claim 14, further comprising:

(a) disposing a second substrate on the sealing resin after forming the wire inside the through hole; and

(b) electrically connecting the wire formed inside the through hole and a third metal pattern formed on the second substrate to each other.

19. A method according to claim 14, wherein said placing a semiconductor chip includes placing a plurality of semiconductor chips on the upper surface of the substrate, the method further comprising:

separating the plurality of semiconductor chips from each other to obtain a plurality of semiconductor packages after forming the wire inside the through hole

20. A method according to claim 14, further comprising:

(a) forming a fourth wire on the surface of the sealing resin after forming the wire inside the through hole, the fourth wire being electrically connected to one end of the wire;

(b) forming an insulating layer on the fourth wire; and

(c) forming a third electrode which is electrically connected to the fourth wire and exposed from the insulating layer.

21. A method according to claim 16, further comprising:

(a) disposing a second substrate on the sealing resin after forming the wire inside the through hole; and

(b) electrically connecting the wire formed inside the through hole and a third metal pattern formed on the second substrate to each other.

22. A method according to claim 16, wherein said placing a semiconductor chip includes placing a plurality of semiconductor chips on the upper surface of the substrate, the method further comprising:

separating the plurality of semiconductor chips from each other to obtain a plurality of semiconductor packages after forming the wire inside the through hole.

23. A method according to claim 16, further comprising:

(a) forming a fourth wire on the surface of the sealing resin after forming the wire inside the through hole, the fourth wire being electrically connected to one end of the wire;

(b) forming an insulating layer on the fourth wire; and

(c) forming a third electrode which is electrically connected to the fourth wire and exposed from the insulating layer.